Listing of the Claims

1. (Previously Presented) A liquid crystal display system, comprising:

a liquid crystal display panel including a plurality of data lines,

a plurality of gate lines intersecting the data lines, and a plurality of pixel electrodes arranged in a matrix type and each having a switch connected to one of the gate lines and one of the data lines;

a gate driver for successively applying a gate voltage to the gate lines to turn on the switches;

a data driver for applying a gray voltage, corresponding to image data signals, to the data lines;

a timing controller for sending both the image data signals and a shift clock signal to the data driver,

a first signal wire adjacent to a ground surface area through which the shift clock signal is transmitted to said data driver; and

a second signal wire through which a first clock signal having a frequency equal to the shift clock signal but having a phase difference of 90° to 270° is transmitted to the ground surface area through a resistor, the second signal wire being a direct current connection to ground surface area through the resistor, the first clock signal being generated in the timing controller, the first signal wire and the second signal wire being formed in parallel.

2. (Cancelled)

3. (Cancelled)

4. (Previously Presented) The liquid crystal display system of claim 1, wherein the first signal wire and the second signal wire are provided on a circuit board.

5 . (Previously Presented) The liquid crystal display system of claim 4, wherein the circuit board is a multi-layered printed circuit board and the first signal wire and the second signal wire are formed in parallel on the same layer.

6. (Previously Presented) The liquid crystal display system of claim 4, wherein the circuit board is a multilayered printed circuit board and the first signal wire and the second signal wire are formed on different layers.

7. (Previously Presented) The liquid crystal display system of claim 1, wherein the first clock signal has 180° phase difference from the shift clock signal.

8. (Previously Presented) The liquid crystal display system of claim 7,

wherein the data driver comprises a plurality of data driver integrated circuits for receiving the image data signals and the shift clock signal from the timing controller and applying the gray voltage corresponding to the image data signals to the data lines of the LCD panel.

9. (Previously Presented) The liquid crystal display system of claim 8, wherein the data driver integrated circuits comprise:

a shift register for shifting and storing the image data signals in synchronization with the shift clock signal after receiving the image data signals from the timing controller;

a D/A converter receiving the image data signals stored in the shift register and converting the image data signals to a corresponding grey voltage; and

an output buffer for temporarily storing the gray voltage output from the D/A converter, and applying the gray voltage to the data lines of the liquid crystal display panel line by line.

10. (Previously Presented) A liquid crystal display system, comprising:

a liquid crystal display panel including a plurality of data lines, a plurality of gate lines intersecting the data lines, and a plurality of pixel electrodes arranged in a matrix type and each having a switch connected to one of the gate lines and one of the data lines;

a gate driver for successively applying a gate voltage to the gate lines to turn on the switches;

a circuit board including:

a timing controller for generating a first image data signal and a second image data signal and generating a first shift clock signal and a second shift clock signal with a phase difference of 90° to 270° that respectively shift the first image data signal and the second image data signal;

a first image data signal wire and a second image data signal wire through which the first image signal and the second data signal are respectively transmitted; and

a first shift clock signal wire and a second shift clock signal wire through which the first shift clock signal and the second shift clock signal are respectively transmitted, the second shift clock signal wire being a direct current connection to a resistor directly connected to ground, the first shift clock signal wire and the second shift clock signal wire being formed in parallel;

a data driver receiving the first image data signal and the second image data signal and the first shift clock signal and the second shift clock signal from the timing controller,

and applying a gray voltage corresponding to the first image data signal and the second image data signal to the data lines.

11. (Previously Presented) The liquid crystal display system of claim 10/ wherein the first image data signals are odd image data signals, and the second image data signals are even image data signals.

12. (Original) The liquid crystal display system of claim 10/ wherein the first shift clock signal and the second shift clock signal have a phase shift of 180°.

13. (Original) The liquid crystal display system of claim 12, wherein the first image data signal and the second image data signal have a phase shift of 90° to 270°.

14. (Previously Presented) The liquid crystal display system of claim 13, wherein the first image data signal and the second image data signal have a phase difference of 180°.

15. (Previously Presented) The liquid crystal display system of claim 14/ wherein the first image data signal is synchronized to a rising edge of the first shift clock signal, and the second image data signals signal is synchronized to a falling edge of the second shift clock signal.

16. (Previously Presented) The liquid crystal display system of claim 14,

wherein a pulse width of the first shift clock signal and the second shift clock signal falls within the interval of a high signal or a low signal of the odd image data signal and the even image data signal.

17. (Previously Presented) The liquid crystal display system of claim 13, wherein the first image data signal and the second image data signal have a phase difference of 90° or 270° .

18. (Previously Presented) The liquid crystal display system of claim 1, wherein the first clock signal transmitted to the ground is effective to offset electromagnetic interference (EMI) caused by the transmission of the shift clock signal.

19. (Previously Presented) The liquid crystal display system of claim 18, wherein the ground has a ground surface, the first clock signal transmitted to the ground being effective to reduce current fluctuation on the ground surface.

20. (Previously Presented) The liquid crystal display system of claim 10, wherein the second shift clock signal transmitted to the ground is effective to offset electromagnetic interference (EMI) caused by the transmission of the first shift clock signal.

21. (Previously Presented) The liquid crystal display system of claim 20, wherein the ground has a ground surface, the first shift clock signal transmitted to the ground being effective to reduce current fluctuation on the ground surface.

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